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| TRANSMITTAL FORM (to be used for all correspondence after initial filing) | Application Number | 10 / 697,133 | |
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| | First Named Inventor | Philip | |
| | Art Unit | | |
| | Examiner Name | | |
| Total Number of Pages in This Submission | 12 | Attorney Docket Number | PST |

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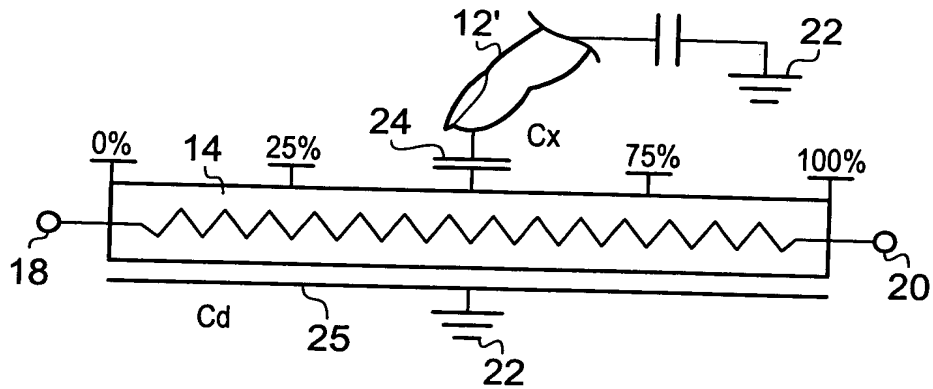


Fig. 1

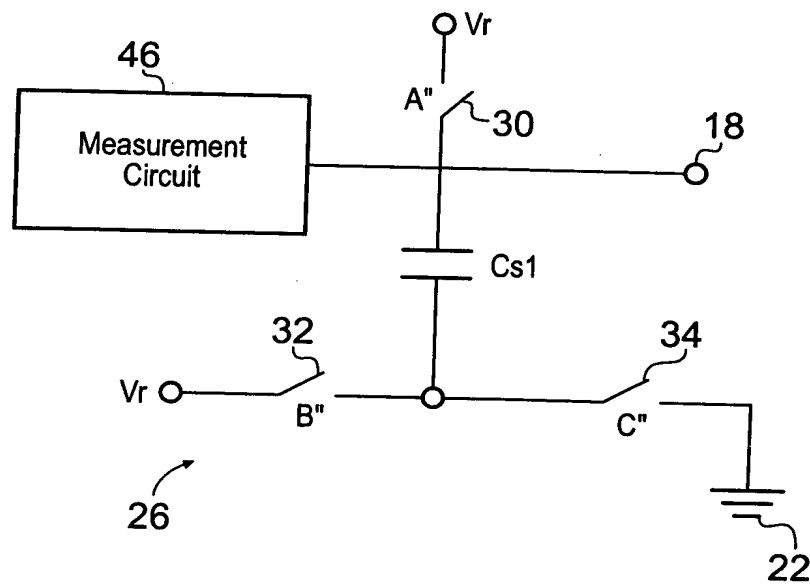


Fig. 2c

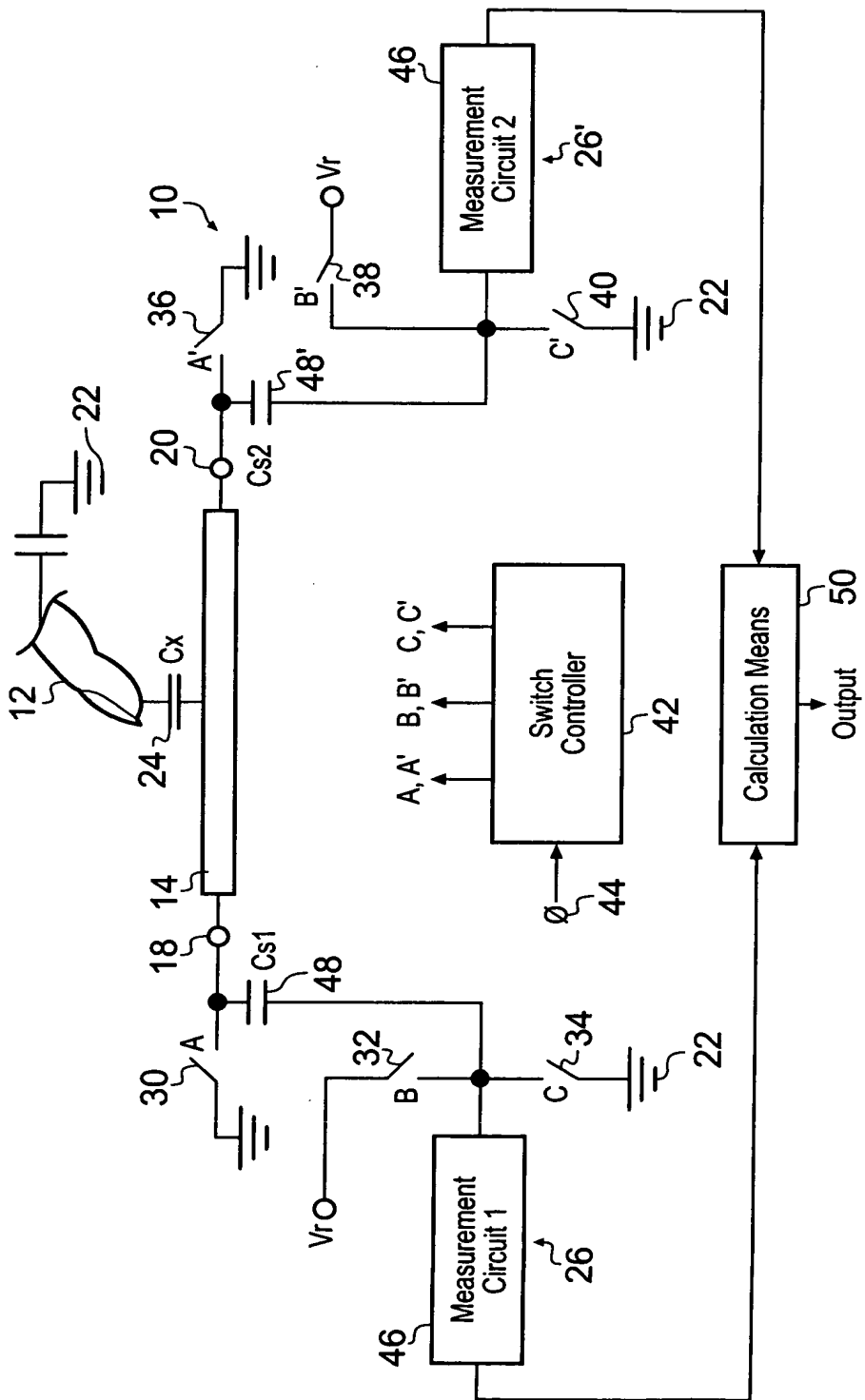


Fig. 2a

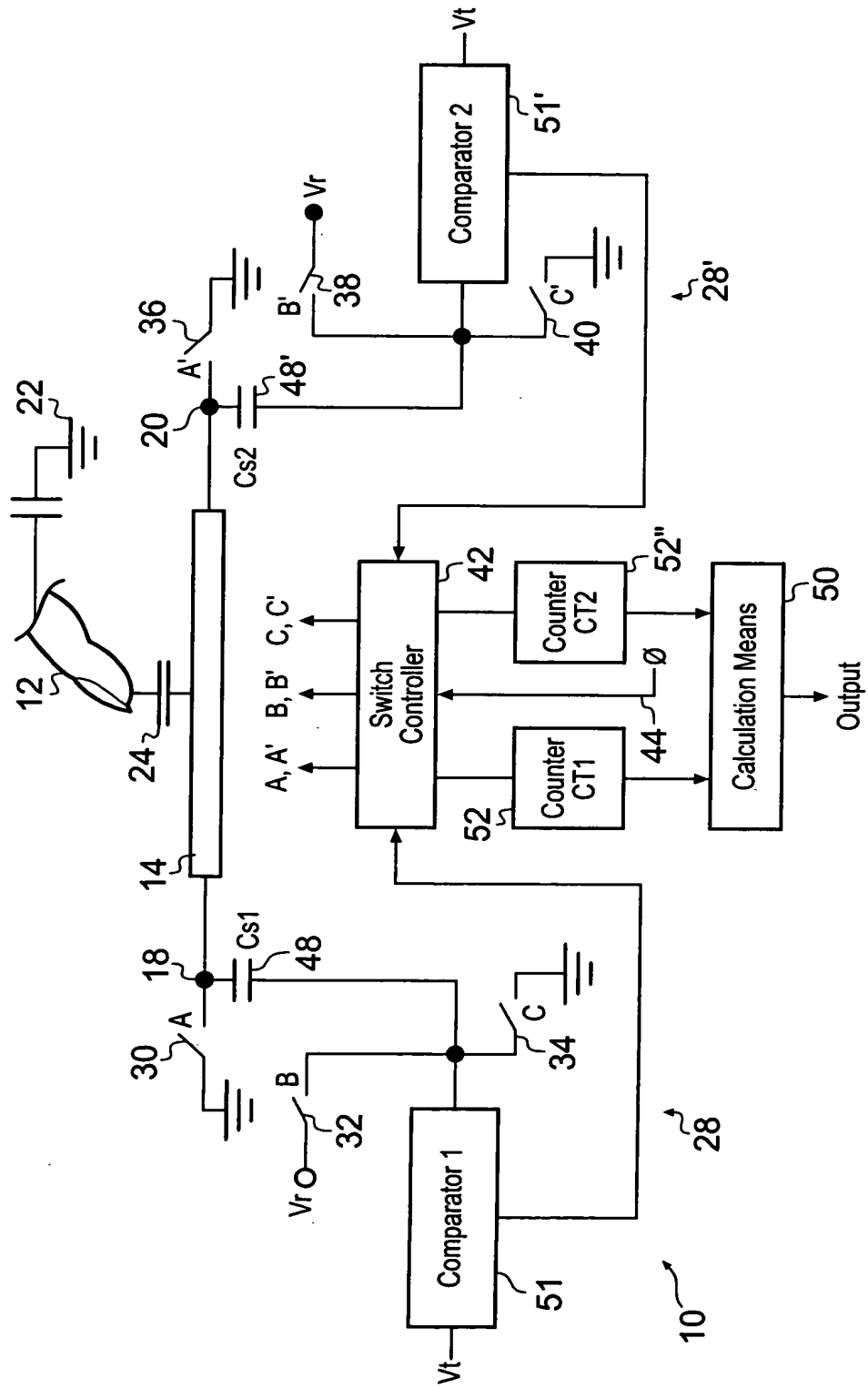


Fig. 2b

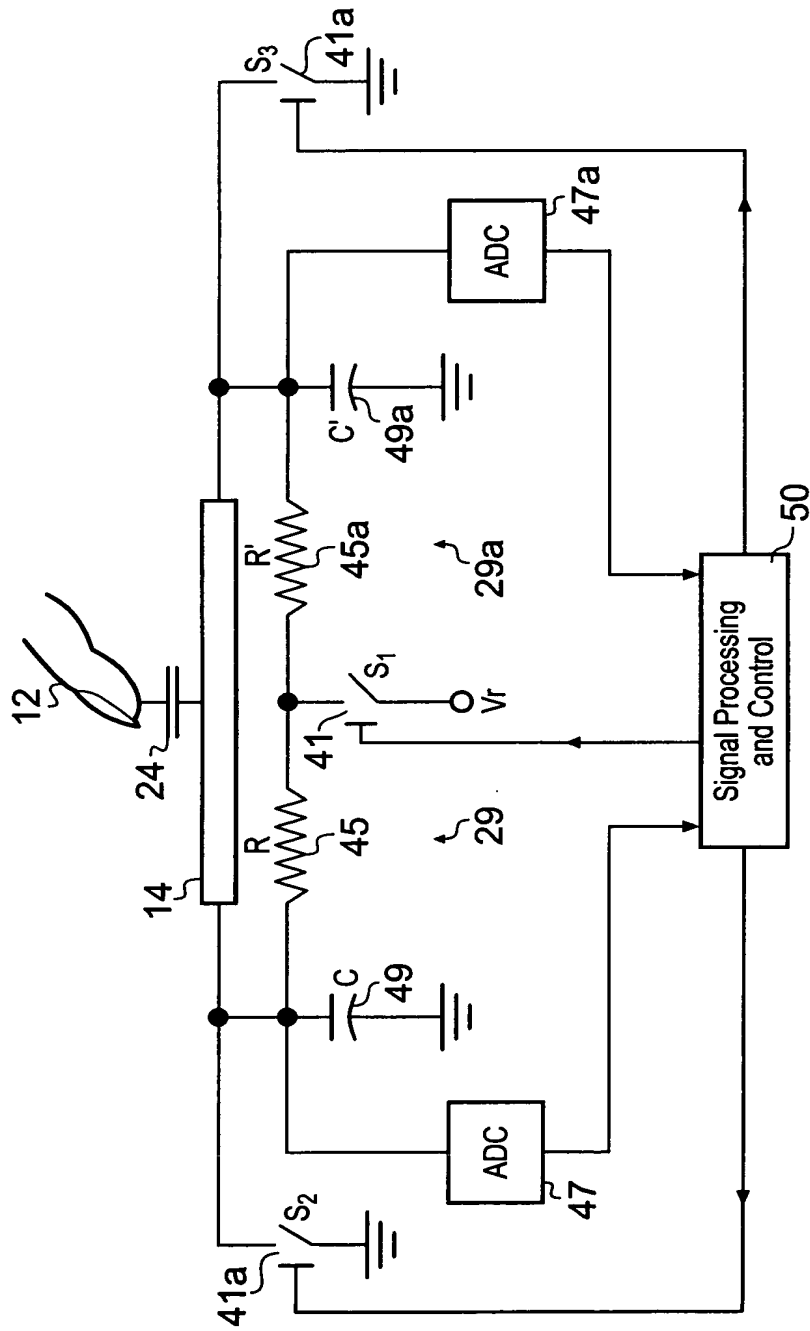


Fig. 2d

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Switching Sequence of A, A', B, B', C, C' for Figure 2A

- 1 Close A, A', C, C' (reset Cs1, Cs2)
- 2 Float all switches
- 3 Close B, B' (charge Cs1, Cs2)
- 4 Float all switches
- 5 Close A, A' (clamp strip to ground)
- 6 Measure 1, 2
- 7 goto step 1 (if desired)

Fig. 3A

Switching Sequence of A, A', B, B', C, C' for Figure 2B

- 1 Reset Counters CT1, CT2
- 2 Close A, A', C, C' (reset Cs1, Cs2)
- 3 Float all switches
- 4 Close B, B' (charge Cs1, Cs2)
- 5 Float all switches
- 6 Close A, A' (clamp strip to ground)
- 7 If $(VCs1 < V_t)$ then increment CT1;
If $(VCs2 < V_t)$ then increment CT2
- 8 If $((VCs1 < V_t) \text{ or } (VCs2 < V_t))$ then goto step 3
- 9 Float all switches
- 10 goto step 1 to repeat (if desired)

Fig. 3B

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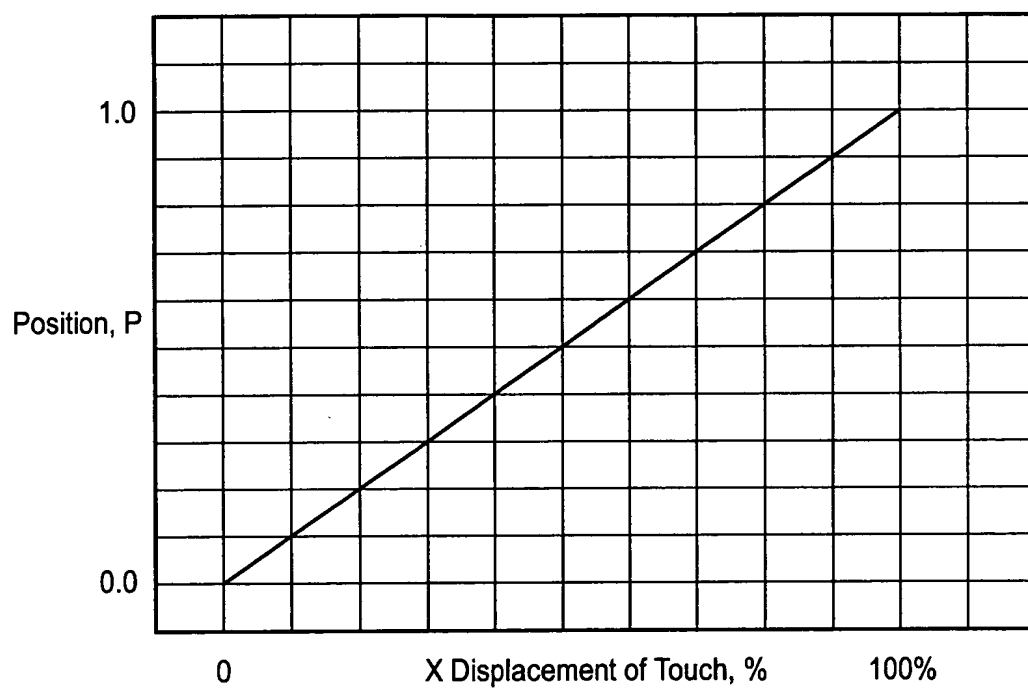


Fig. 4

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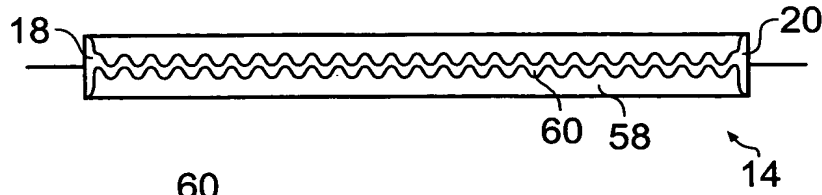


Fig. 5

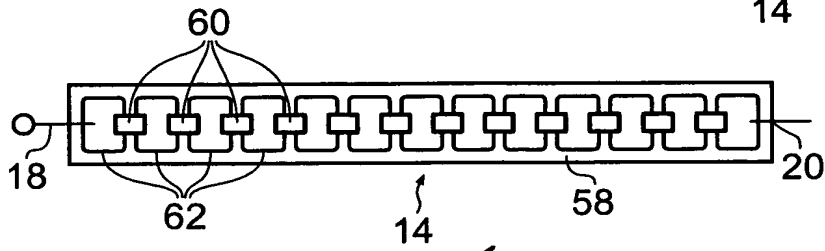


Fig. 6a

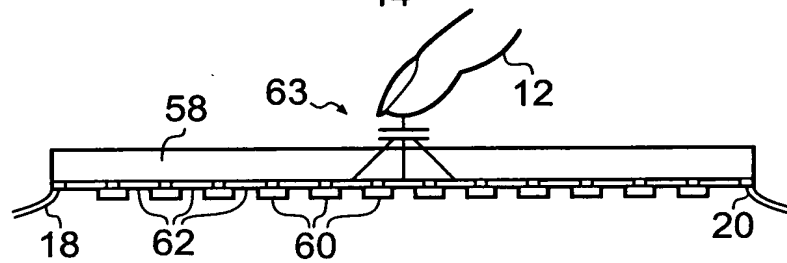


Fig. 6b

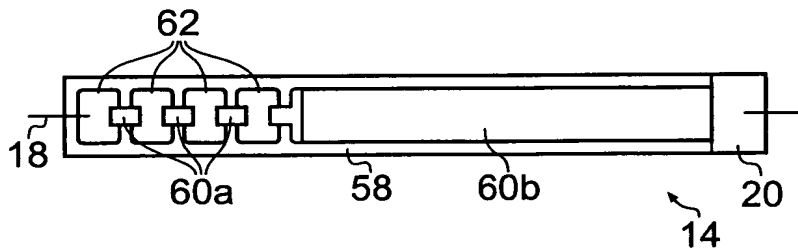


Fig. 7

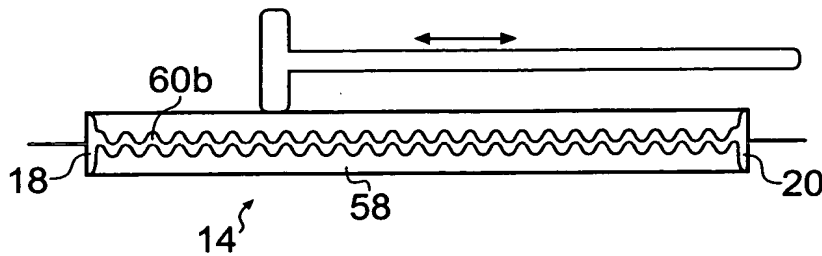


Fig. 9

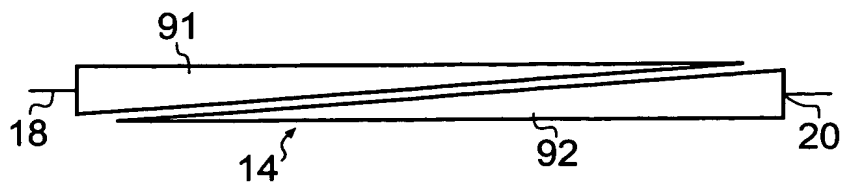


Fig. 15

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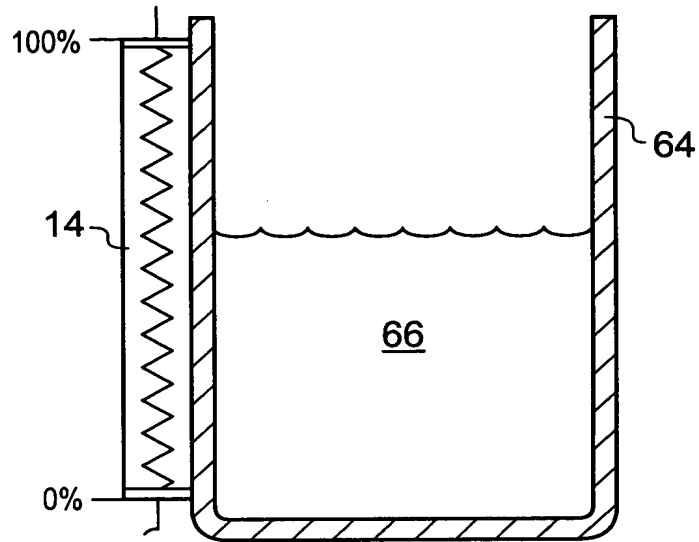


Fig. 8a

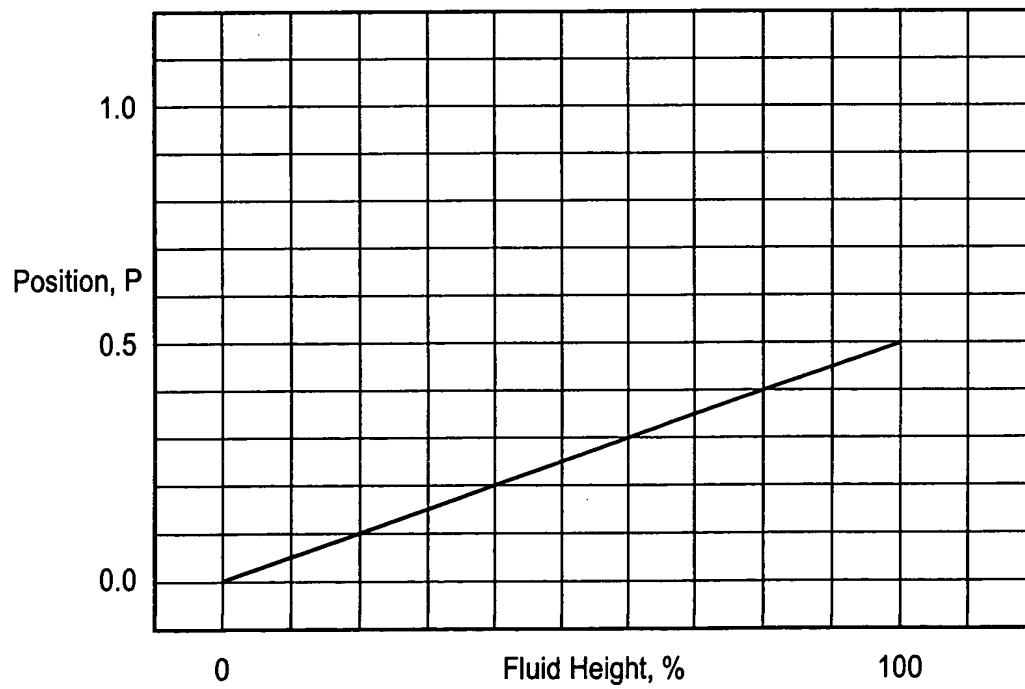


Fig. 8b

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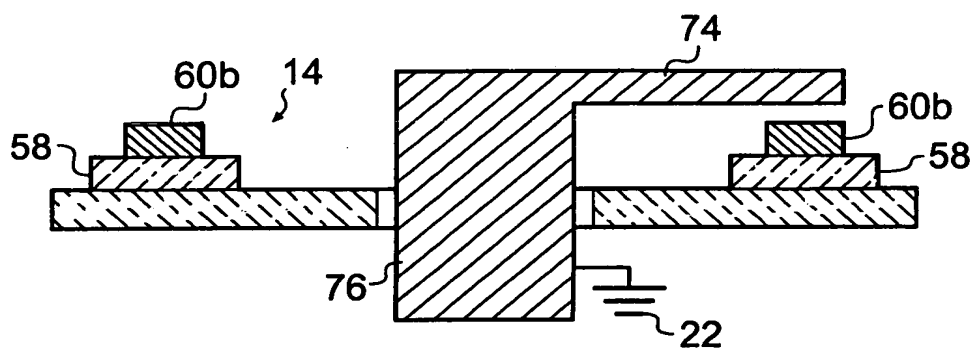
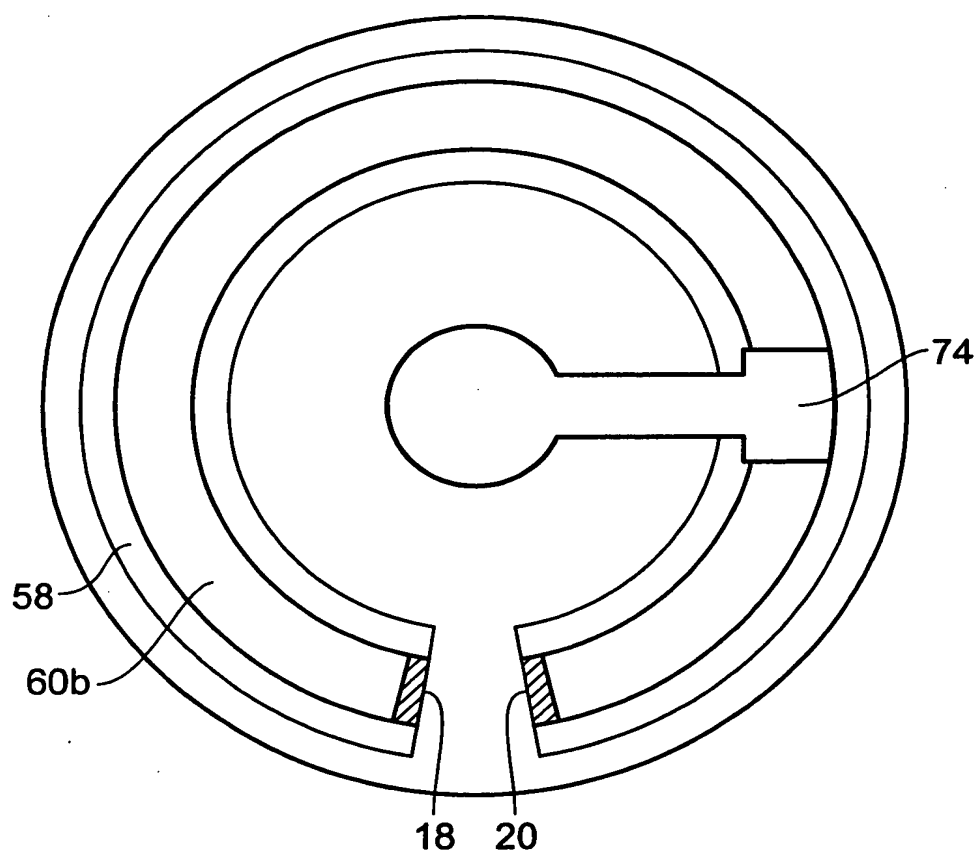


Fig. 10b

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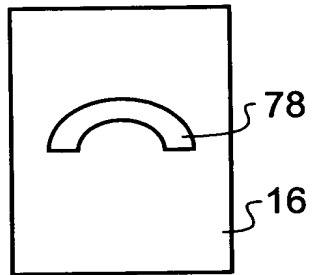


Fig. 11

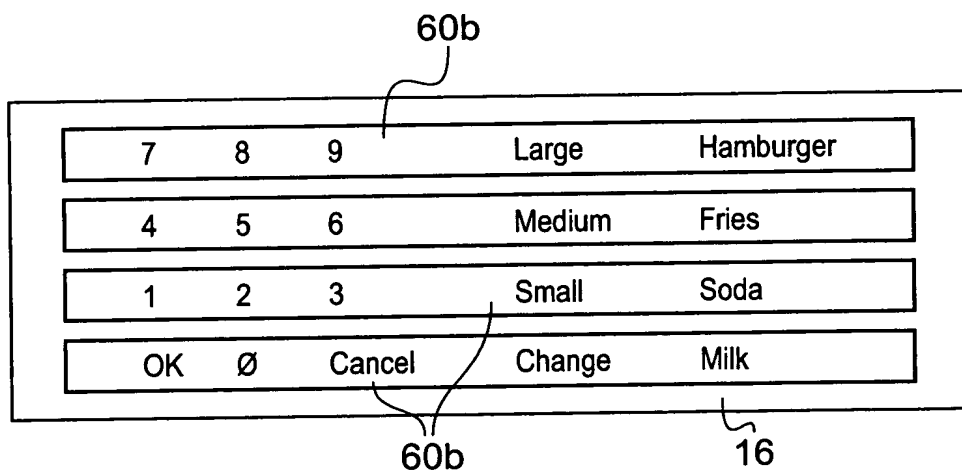


Fig. 12

Block diagram of a control system 90. An MCU is connected to a coil 14. The MCU has two outputs: 'Serial Output' and 'PMW Output'. It also has four I/O pins: I/O (A'), I/O (B', C'), I/O B, C, and I/O A. I/O (A') is connected to one terminal of capacitor CS2 (48'). I/O (B', C') is connected to the other terminal of capacitor CS2 (48'). I/O B, C is connected to one terminal of capacitor CS1 (48). I/O A is connected to the other terminal of capacitor CS1 (48). The capacitors CS1 and CS2 are connected in series to the coil 14.

Fig. 14